THERMAL NEEDS AND CHALLENGES IN NEXT GENERATION SOLID STATE LIGHTING APPLICATIONS: LIGHT EMITTING DIODES

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ASTRACT

Light emitting diodes, LEDs, historically have been used for indicators and produced low amounts of heat. The introduction of high brightness LEDs with white light and monochromatic colors have led to a movement towards general illumination. The increased electrical currents used to drive the LEDs have focused more attention on the thermal paths in the developments of LED power packaging. The luminous efficiency of LEDs is soon expected to reach over 80 lumens/W, this is approximately 6 times the efficiency of a conventional incandescent tungsten bulb. Thermal management for the solid-state lighting applications is a key design parameter for both package and system level. Package and system level thermal management is discussed in separate sections. Effect of chip packages on junction to board thermal resistance was compared for both SiC and Sapphire chips. The higher thermal conductivity of the SiC chip provided about 2 times better thermal performance than the latter, while the under-filled Sapphire chip package can only catch the SiC chip performance. Later, system level thermal management was studied based on established numerical models for a conceptual solid-state lighting system. A conceptual LED illumination system was chosen and CFD models were created to determine the availability and limitations of passive air-cooling.

INTRODUCTION

The introduction of the first practical visible solid state LED occurred in 1962, and was invented by Nick Holonyak of the General Electric Company [Holonyak, 1992]. It was discovered that the

wavelength of an infrared GaAs diode could be shifted to the visible spectrum by the introduction of phosphate dopants. The introduction of a compatible large band gap material raises the overall band gap thus shifting emission into the visible spectrum. The wavelength of an emitted photon can be approximated by;

$$\lambda = \frac{hc}{E_{bg}} \quad (1)$$

Where h represents Planck's constant, c is the velocity of light and E_{bg} is the band gap energy. Thus, raising the band gap of GaAs from 1.4 to 1.9 shifts the emission into the visible red region at approximately 650 nm [Spring et. al, 2003]. These early red devices typically emitted 0.001 lumen per device. Due to their longevity, power requirements, and resistance to shock and vibration the LEDs found uses as indicator and signal applications. Throughout the next two decades advances continued in material development and processing leading to improved efficiency, reliability and additional colors. These advances included changes in elemental proportions, doping and substrate materials resulting in the development of GaAsP LEDs in the orange and yellow portion of the spectrum. During the 1980s refinement of the use of GaAlAs grown on AlGaAs substrates, and multilayer hetero-junction structures in chip fabrication led to an order of magnitude improvement in brightness. Also to appear were AlGaInP on GaAs devices that resulted from the development of organo-metalic vapor phase epitaxy (OMVPE). New materials and techniques enabled high brightness (HB), LEDs from the yellow to red spectrum. During the early 1990s advances were made in OVMPE growth of AlInGaP on GaAs substrates [Maaskant, 2001]. These devices continued to improve quantum efficiencies to 99.9%. The problem, then, was not photon generation but to get the photons out of the LED device. Absorption in the GaAs substrate was a critical problem. Bragg mirrors were incorporated in to the epitaxial structure for improved emission.

In 1994 Hewlett-Packard developed a technique to remove the GaAs substrate by etching. The active layer was then subsequently wafer-bonded to a transparent GaP substrate to form what it is recognizes as TS AlInGaP devices. Ultimately red devices reached efficiencies of 25 lm/W, however a typical LED was still only producing 3 lumens. Soon to follow was the development of AlGaN devices on sapphire by Nakamura et al [1996]. The wider band gap of AlGaN allowed the development of devices in the green, blue and UV wavelengths. A competitive technology developed by CREE utilizes AlGaN grown on semitransparent SiC substrates. Advances in materials, doping and

annealing have resulted in green devices at 30-40% efficiencies, while blue and UV devices have achieved levels of 50-60%. The development of blue LEDs was significant as it allowed the first solid-state white light devices to be produced. One approach uses an appropriate combination of red, green and blue LEDs to produce white light, while the second approach utilizes a blue or UV LED and a phosphor to create white light. Early 5mm devices utilizing a blue LED and yellow phosphor attained levels of 1-2 lumens per device at 10-15 lm/W.

To satisfy the niche illumination needs the efficiency and lumens per device would need to be improved. This would require enhanced device materials, phosphors, and larger LEDs that could be driven at higher currents while maintaining efficiency. In the late 1990s Lumileds [Lumileds, 2003] introduced the first commercial high power LED. This 1W, 1 mm^2 LED operated at 20 times the power level of a conventional 5 mm LED, while approaching twice the efficiency of an incandescent lamp (~15 lm/W).

White LEDs can exhibit exceptional lifetimes, exceeding 50000 hrs, when operated under ideal conditions. Unlike an incandescent bulb filament operating at over 1000 °C, an LED device junction temperature should be kept under 120 °C. In order to meet this requirement the package and system materials and thermal design become crucial. Unlike traditional 5 mm devices with a package thermal resistance of 300-400 K/W, a power LED package resistance needs to be less than 20 K/W. At elevated temperatures the lumen depreciation with time is enhanced and performance is degraded. The effects on all of the package components such as; chip, wire-bonds, encapsulation, lens, lead-frame over-mold, and submount material must be considered.

The choice of materials in the optical extraction path of the package is also very important. Most plastics or epoxies degrade or darken with exposure to UV radiation. This degradation is permanent and greatly enhanced with increased temperature in the package. To minimize this effect, the thermal path out of the package is directed away from the optical path. With shorter wavelength UV devices the degradation becomes even a larger concern. Thermal rise within the package can also exert stress on the package assembly due to the CTE mismatch of the various components. This becomes a problem when the device is continuously power cycled causing separation of the package materials. Ultimately catastrophic wire bond failures may occur.

Technological advances in the microelectronics industry have led to a rapid increase in the transistor density and speed of conventional electronic chips, and hence an increase in the dissipated heat fluxes. Based on the recent NEMI Packaging Technology Roadmap, it may be anticipated that a single microprocessor chip may reach heat fluxes in excess of 150 W/cm^2 by 2012 [NEMI Report,

2002]. A typical LED power-package has a 1 mm^2 surface area with a total heat generation of 1 W corresponding to a heat flux of 100 W/cm^2 [Arik et.al, 2002]. With increased temperature several effects can be observed in LEDs. Increasing junction temperature lowers the overall efficiency of the device, lowers the forward voltage, causes the emission to shift to longer wavelengths, and reduces the device lifetime and reliability. The reduction in efficiency and shift in wavelength will cause the color temperature to change especially in blue-based white LED devices. Additionally a rise in the phosphor's temperature reduces the quantum efficiency thus reducing lumen output. Wavelength shift and phosphor efficiency represent a reduction in the device performance. Lifetime effects due to temperature conditions are not reversible. These effects may exhibit themselves as changes in the electrical performance or reduced output. Although not fully understood, increased degradation with increased temperature has been clearly correlated. Current crowding and high crystal defect density relating to metal migration, at high temperatures and voltage, along defect tubes have been blamed [Maaskant, 2001]. It is clear that thermal management of high power LEDs is crucial to long-term reliability.

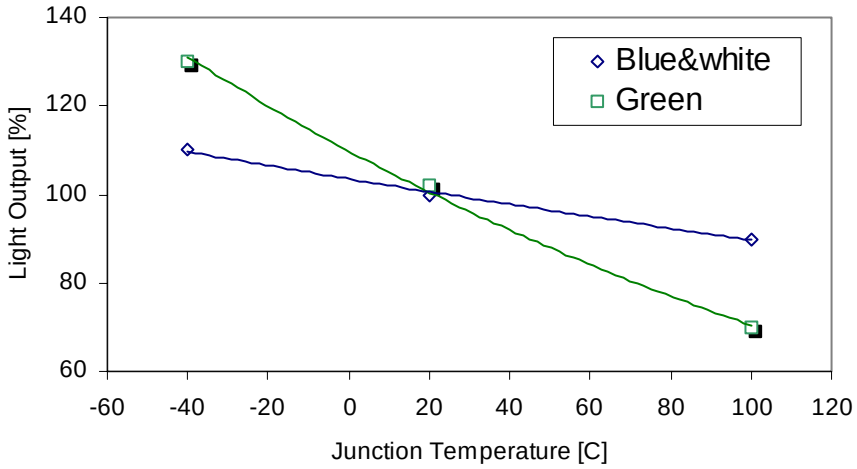

Figure 1. Variation of the light output with the junction temperature [Arik et al, 2002]

Both package and system level thermal management is discussed in this paper. Unfortunately, not all of the thermal issues were included in the discussions due to space limitations, but vital parts are included with supported numerical models of both conduction and convection based problems.

THERMAL MANAGEMENT OF SOLID STATE LIGHTING DEVICES

Although it is a fairly new market, LEDs as an alternative to conventional lighting products, brings some demanding thermal challenges. A typical LED lighting system is faced with the issues of decreasing the thermal resistance from junction to the substrate, and the availability of the orientation independent, cost-effective system level thermal solutions. The efficiency of solid-state lighting devices strongly depends on the junction temperature as given in Figure 1. A strong argument by solid state lighting advocates is the long life of the LEDs, which results in cheaper and more reliable illumination systems. Current LEDs are more sensitive to temperature than standard solid-state electronic components so that more attention must be paid to the thermal architecture.

Evolution of the LED technology shows an interesting trend since the invention of the first LED. Since LED usage began with indicator lights and display segments, the primary packaging of die required low driving power. Figure 2 presents the technological milestones for the LED technology spanning the range of low power to high brightness systems. With the invention of high brightness LEDs, interest in higher driving currents and greater power dissipation began. First generation high brightness chips, rated at 80 mW, were packaged in 5 mm systems. These packages can be over-driven to higher currents but with a thermal resistance of approximately over 250 K/W, removing heat from the chip has become very challenging.

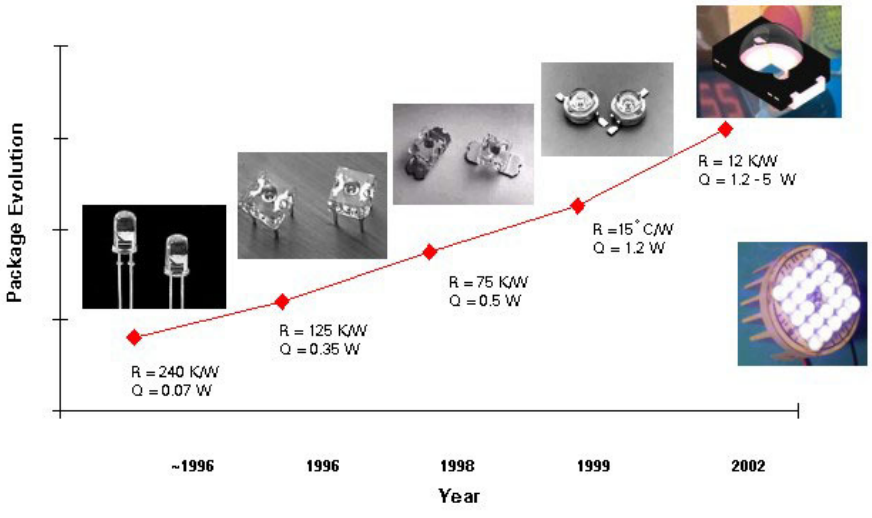

Figure 2. LED packaging technology evolution by years

A typical LED illumination system has multiple HB packages, which are attached to a substrate located on a heat sink. Figure 3 presents a typical LED illumination system. As it can be seen from the figure, the heat sink has very limited footprint area and volume due to the tight boundaries of the system. Heat is conducted through the multiple metallic/non-metallic parts of the package, interface materials, heat sink, and is eventually rejected through convective heat transfer to the ambient environment.

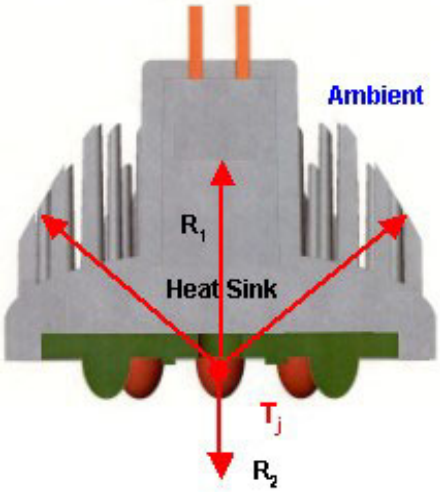

Figure 3. A typical LED illumination system

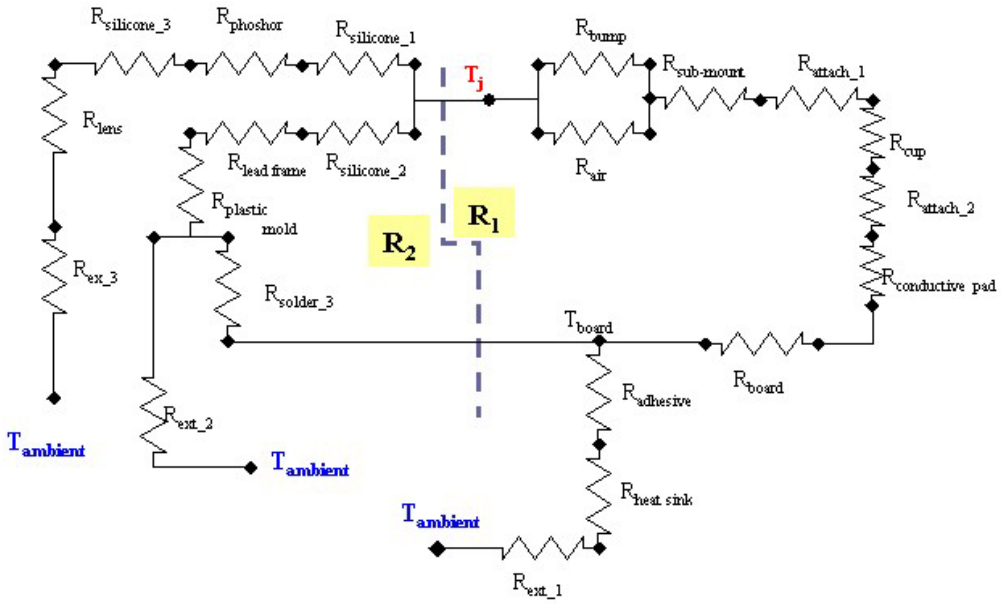

Figure 4. Typical resistance network for an LED illumination system

A close examination of a typical LED illumination system will provide individual components of the thermal structure. A simplified resistance network between the chip junction and the ambient is given in Figure 4. This simplified electrical analogy provides two main components of the heat transfer path. While R_1 is given as the path between the junction and the ambient via en extended surface, the R_2 path is towards the upper side of the chip. Over twenty resistances define the thermal behavior of the system.

Combination of two parallel resistances creates an LED system as presented in Figure 4. Total thermal resistance between the chip junction and the ambient can be given as follows:

$$\frac{1}{R_{junction-ambient}} = \frac{1}{R_1} + \frac{1}{R_2} \qquad (2)$$

Due to the low thermal conductivities of epoxy, silicone and phosphor, the total thermal resistance between the junction and the topside of the chip, R_2, is very large in comparison with the well-engineered junction to heat sink side (i.e. $R_2 >> R_1$). Therefore, heat transfer towards the topside can be negligible. A Finite Element Model (i.e. FEM) was also established to understand this behavior. A high brightness chip was located in a metallic frame, which is filled with light transparent non-metallic material. The plastic-molded package was then attached to a thermally conductive substrate. A constant heat load at the chip active layer, and an external convection boundary condition at the conductive substrate, was applied. A natural convection boundary layer was applied at the lens external surface to obtain the heat transfer effect, and numerical models were run to determine the temperature gradients.

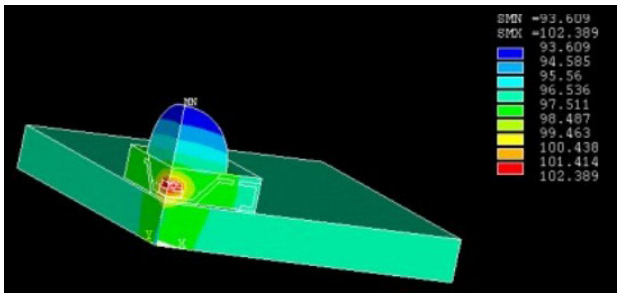

Figure 5. A typical LED system with heat transfer from lens side

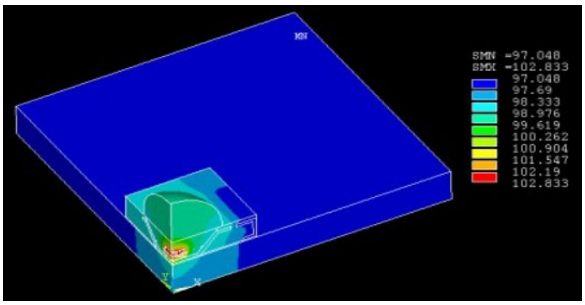

Figure 6. A typical LED system without heat transfer from lens side

Figure 5 presents the numerical findings for the natural convection from the lens outer surfaces. The LED junction temperature was found to be 102.4 °C while the minimum temperature is 93.6 °C at the lens. Figure 6 shows no convection at the lens. In that case, the maximum chip temperature was found to be 102.8 °C, while the minimum temperature is 97.1 °C. It is noticeable that the junction temperature only changed 0.4 °C corresponding to a 0.3 percent change. Design constraints in LED applications would not usually allow heat transfer from lens side, even if available, it would be a negligible temperature effect.

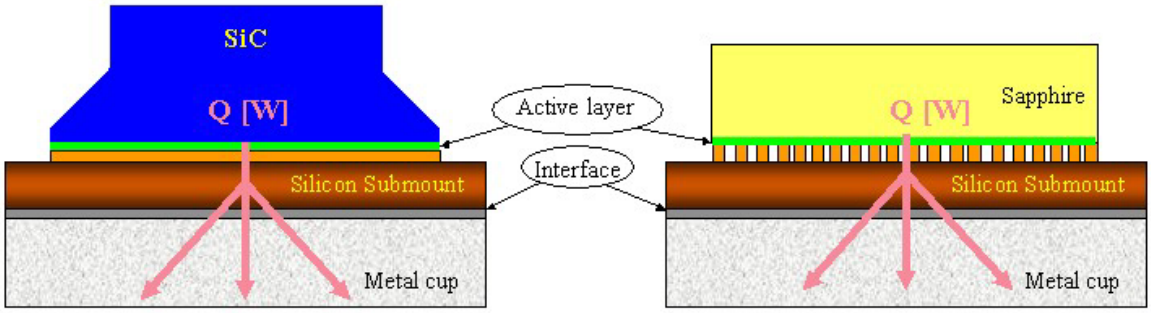

Figure 7. Schematic diagram of two packages with different chips and layouts

PACKAGE LEVEL THERMAL MANAGEMENT

Various chips in HB LEDs are fabricated with materials ranging from low conductivity Sapphire to high conductivity SiC. A typical flip chip LED has the active layer down, attached to a silicon sub-mount. This assembly is then placed into a metal cup having a conical housing. Later the open space is filled with a transparent material. This structure is usually attached to a metallic board that will later be connected to a heat sink. Given the series of thermal resistances, neglecting the constriction resistances, system components such as; chip, bump/continuous layer, sub-mount, metal cup, attachments, and interface layers have significant effects on the package thermal behavior. Geometry and material properties of each component as well as surface characteristics contribute to the thermal performance. To compare the effects of chip material, and designated bump structure FEM models were created.

Figure 7 presents the two systems with SiC and sapphire chips on the same platform. Except for chip bump layout and submount design, both chips have the same metal frame and

package architecture. Heat generation was applied at the chip active layer, and the steady state energy equation was solved for a convective boundary condition. A fine mesh structure in the numerical model was created with an adequate number of elements. Figure 8 presents the numerical findings for both cases. The maximum junction temperature in the SiC chip was found to be 120 °C, and the corresponding junction to board thermal resistance is approximately 4.4 K/W. Meanwhile, the sapphire chip performance was not as good as the SiC chip system. The maximum chip temperature was found to be 124.1 °C, which resulted in a junction to board thermal resistance of 9.2 K/W. There are two particular reasons for this; the low thermal conductivity of sapphire and the bump layout.

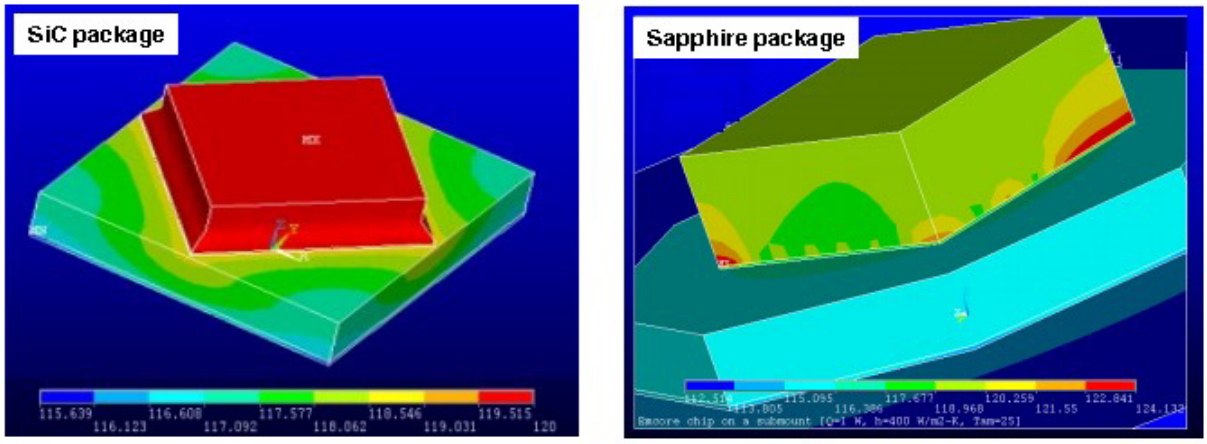

Figure 8. Temperature distribution in both SiC and Sapphire chip packages

Table 1. Summary of the numerical findings

	SiC Package			Sapphire Package		
Component	T_{max} [°C]	T_{min} [°C]	ΔT [°C]	T_{max} [°C]	T_{min} [°C]	ΔT [°C]
Chip	120.1	119.5	0.6	124.1	117.7	6.4
Attachment	120.1	118.7	1.4	118.8	117.5	1.3
Submount	119.7	116.5	3.2	118.7	115.2	3.5

Further investigation was carried out to understand the lower thermal performance of the sapphire system. Although the Sapphire chip package had a thermally better chip to submount attachment material, due to the local spreading in the active layer, higher temperature gradients were found. Figure 9 presents the temperature gradients in both the bump and submount for the Sapphire chip package.

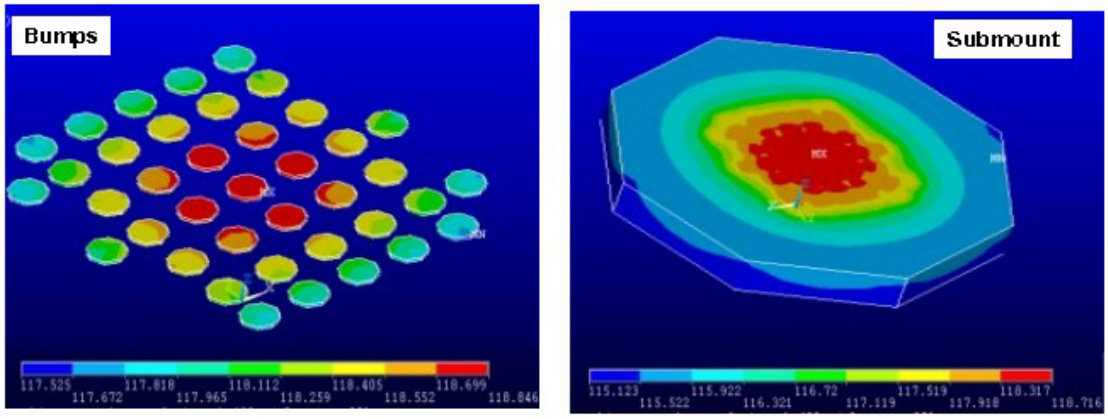

Figure 9. Temperature distribution in the bumps and submount for Sapphire chip package

The results of the numerical study are summarized in Table 1. It can be seen from the table, the dominating resistance in SiC system is the submount, while in the Sapphire system the chip has the strongest influence in the overall thermal resistance.

A further improvement for the Sapphire chip package can be implemented by adding thermally conductive adhesive filler between the chip and the submount. Besides thermal improvement, the adhesive layer will also improve the structural integrity and reliability of the package. The numerical model was revised, and an adhesive layer with a very low thermal conductivity (i.e. 2.5 W/m-K) was added to obtain the thermal performance. Figure 10 presents the temperature plots for both cases. The maximum chip temperatures were found to be 124.1 °C and 120 °C respectively. A 4 °C performance improvement was observed when underfill was applied in the system. The thermal resistance was also improved to 5.2 K/W, which is 4 K/W lower than the “no underfill” package.

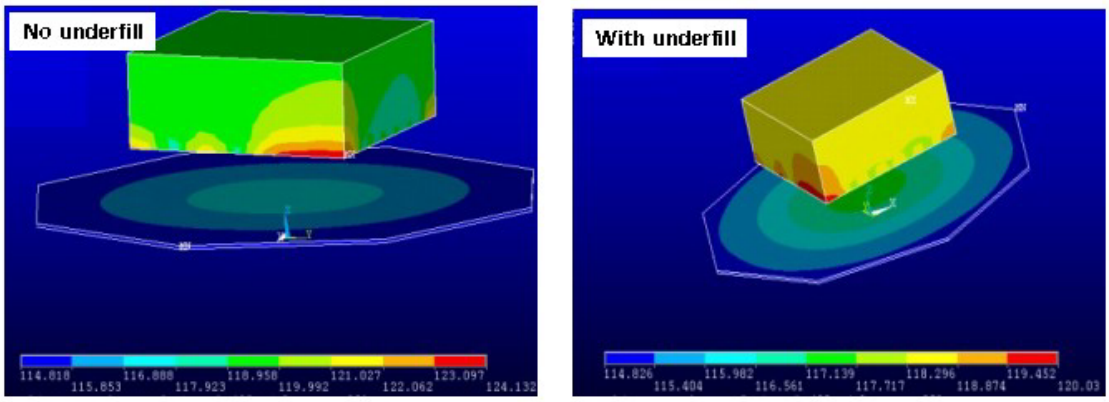

Figure 10. Effect of underfill material on thermal performance of the Sapphire chip package

Experimental studies showed that there is a decrease of approximately 40 percent light output due to high temperature effects on the phosphor particles in HB LED packages. Therefore, a numerical study through FE techniques to investigate the localized heating effects for various phosphor applications was performed. Figure 11 presents the findings for both particles and layers of phosphor in LED packages. Although this is a very generalized model, it demonstrates the local thermal behavior. Coupling the thermal an optical models would create a more sophisticated representation. Results showed that a 3 mW heat generation on a 20 μm diameter spherical phosphor particle could result in excessive temperatures. Due to the low thermal conductivity of the silicone filler, local hot spots may occur. However higher thermal conductivity silicone, if optically feasible, could eliminate this problem. An extensive discussion of reduced quantum efficiency in light conversion phosphor particles due to localized hot spots is given by Arik et al [2003].

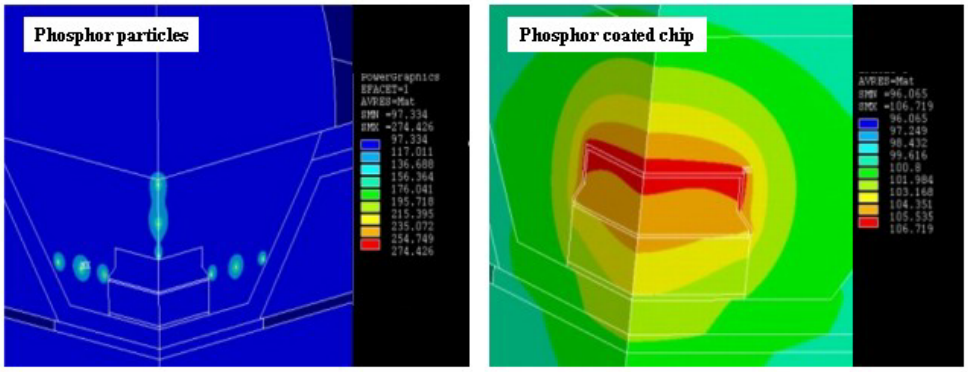

Figure 11. Thermal effects on phosphor particles and layers in LED packages [Arik et al, 2003]

SYSTEM LEVEL THERMAL MANAGEMENT

Current high brightness LED designs have begun to migrate away from 5 mm lamp style packaging into custom packages better designed for heat transfer. The required low junction temperature of the LED demands thermally efficient systems design. For example, a 10 W system in a 50 °C ambient environment with a design goal of 100°C at the heat sink base requires a 5 K/W heat sink resistance. This resistance normally has to be achieved with low cost, passive, orientation insensitive, and reliable solutions. Typical incandescent lighting systems use both radiation and natural convection to achieve successful thermal management. Due to extremely high filament temperatures (~1000 °C), thermal radiation is dominant. On the other hand, solid-state lighting systems are different than conventional lighting systems due to tight junction temperature requirements (Tj $\leq$120 °C). Therefore a typical thermal design for an LED system revolves around efficient LED packaging, and an efficient heat transfer to ambient.

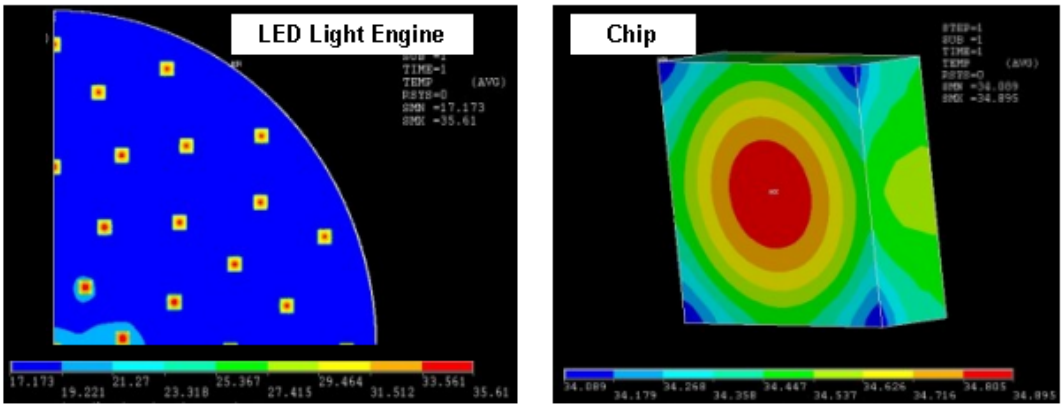

Figure 12. A typical LED light engine, quarter symmetry model

Some lighting systems may need to rely on active cooling or a large conductive sink with passive cooling, but this is not the usual case for lighting applications. The best option, if enough thermal cooling capacity can be achieved, is to use passive cooling methods. Although passive cooling offers the lowest cost, unfortunately it is also the lowest thermal performance of any heat removal technique. As convection is the primary method, much attention needs to

be focused on effective surface area and orientation. LED packages must successfully conduct heat away from the chip to the heat sink. Standard heat sink materials with conductivities of 75 to 200 W/m-K are suitable for system level thermal management. Often, if a material with a lower thermal conductivity is used due to cost or manufacturing reasons, the design will demand either shortening the length of the path or increasing the heat transfer area. Sometimes the conduction part of the thermal path consists of several parts that are held together in various ways. These joints between parts create solid-to-solid thermal interfaces causing additional thermal contact resistances. Surface finishes of each part and the contact pressures are the primary variables that affect the thermal interface resistances. Silicone based gap-filling, thermally conductive epoxy or phase change materials may be used to create intimate contact.

To further understand the thermal needs of an LED illumination system; a conceptual design was developed for a light engine to produce over 1500 lumens. As has been discussed so far, the thermal design can be interactively divided into two parts; the package and the system level thermal management. Assume that package level thermal design results in a 17 °C temperature rise for 1 W at the active region of the chip. Since the design needs to keep the junction temperature at or below 120 °C, the board temperature should not exceed 103 °C. Figure 12 presents a typical LED light engine temperature gradient on both the board and the chip. It is noticeable that the chip does not have considerable temperature gradients (i.e. <1 °C) due to high thermal conductivity of the chip substrate, while the chip to heat sink structure has a considerable temperature gradient. Another interesting finding was that the chips were thermally isolated. In other words, thermal interactions of the chips are limited due to low thermal performance of the dielectric layer. A further drop in the temperature is expected in the thermal interface layer between the conductive substrate and the heat sink. Assume that the best thermal interface material is implemented in a very controlled set-up such as; controlled pressure, perfect mating surfaces and no oxidation. By including all of the given thermal design parameters, we can assume that heat sink base temperature should be 95 °C or lower.

Although designing a heat sink methodology is well outlined in many publications [Kraus and Bar-Cohen, 1995], implementing a heat sink into a particular design needs careful attention. Most of the time, first order correlations would not capture the design parameters such as; air flow scheme, chimney effects, surface radiation, air blockage, boundary layer developments, etc. Therefore, the need for sophisticated numerical models is critical.

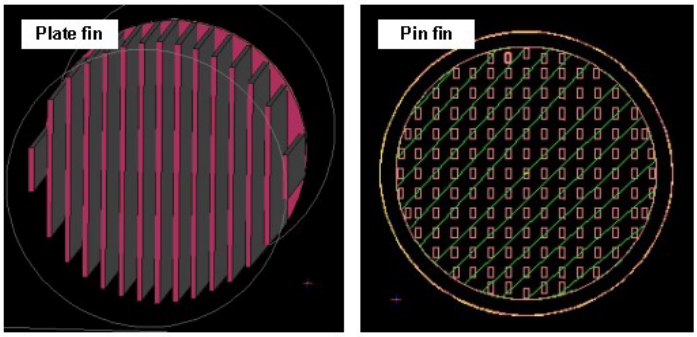

Figure 13. Two fin geometers for the light engine

A numerical CFD model for the light engine given above was created. Various heat sink geometries can be considered under manufacturing constraints. Two fin types, plate and pin fins, are studied in this analysis. Figure 13 presents a close up view of the heat sinks. Both heat sinks have the same footprint area and heights. The material has a thermal conductivity of 177 W/m-K. Numerical models were created using Fluent/Icepak CFD software, which can solve energy, momentum, and continuity equations simultaneously. The number of elements varied between 150000 and 350000 depending on the grid size needs. Typical solution time was between 1-3 h in a multiprocessor SGI workstation.

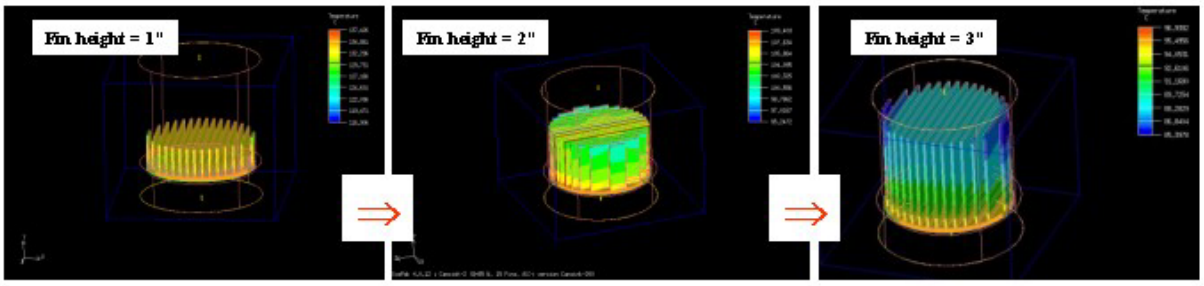

Figure 14. Variation of the fin thermal behavior depend on the fin height

Figure 14 presents the temperature gradients in the plate fin heat sink, which is a common choice for many natural convection air-cooling applications. For the same fin material and number, fin height was varied between 1 and 3 inches to observe the thermal behavior. It can be seen that at lower heights, the heat sink behaved as an isothermal system with higher fin efficiency, while increasing fin height provides a lower heat sink base temperature with lower

fin effectiveness. Variation of the heat sink base maximum temperature, and heat sink to ambient thermal resistance with the fin height is given in Figure 15. The Y-axis at the left represents the temperature, while at the right provides the thermal resistance. A heat sink with 1" fins will have a maximum temperature of 137 °C with a thermal resistance of 1.46 K/W, while 6" fins can provide a base temperature of 81 °C with 0.48 K/W thermal resistances. It is a basic engineering intuition to increase the fin height to remove more heat. However, there are manufacturing constraints for the extrusion, which is known to be the cheapest manufacturing technique for heat sinks. It is also known that fin height to spacing should meet a 10:1 ratio. For the current design it means that fins cannot be taller than 3".

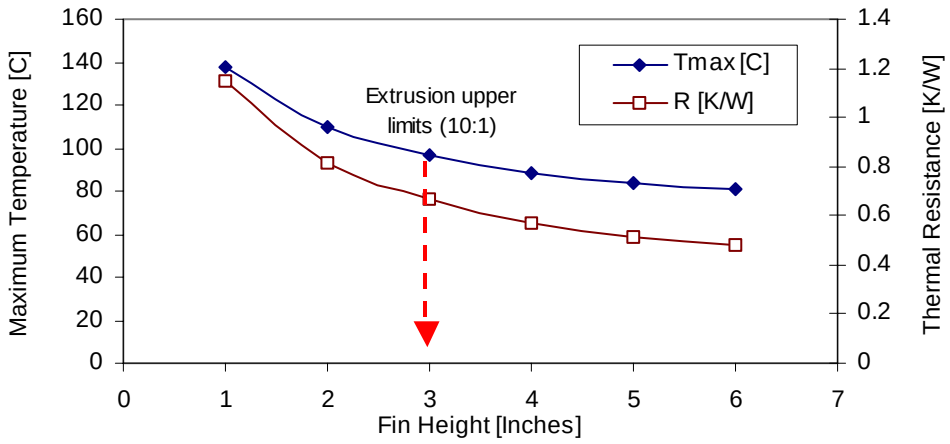

Figure 15. Variation of heat sink maximum temperature and thermal resistance with fin height

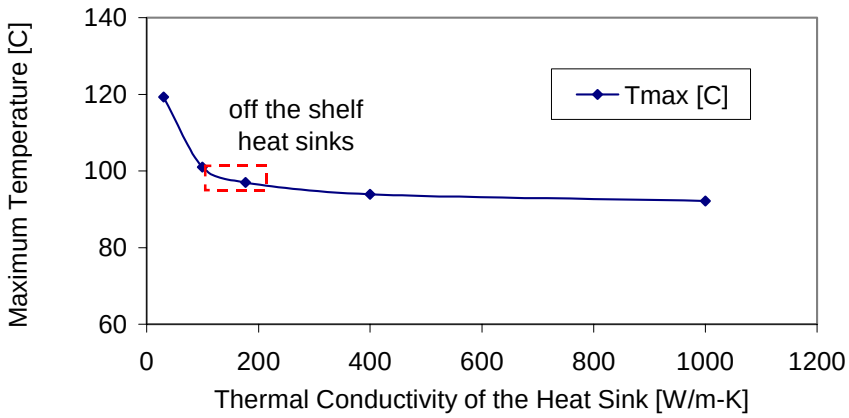

Figure 16. Variation heat sink performance with the material for 3" height fins

The effect of heat sink material was also studied numerically for a 3” height heat sink. Figure 16 presents the heat sink performance as a function of thermal conductivity of the heat sink material. The basic criteria chosen for this analysis manufacturability without the need of more advanced manufacturing techniques such as swaging, forging, or bonding. It can be seen that after 200 W/m-K the heat sink performance barely changes.

The current analysis assumed the heat sink base and fin materials are the same. Some LED applications might require higher thermal conductivity at the base, but lower at the fins. Finally, a comparison between plate and pin fin heat sinks can be made through Figure 17. The plate fin heat sink had a maximum temperature of 96.9 °C, while the pin fin heat sink had 97 °C. One particular reason for this was the spacing for both configurations were very similar. Although the pin fin had better air circulation causing higher heat transfer coefficients, the plate fin had larger available surface area.

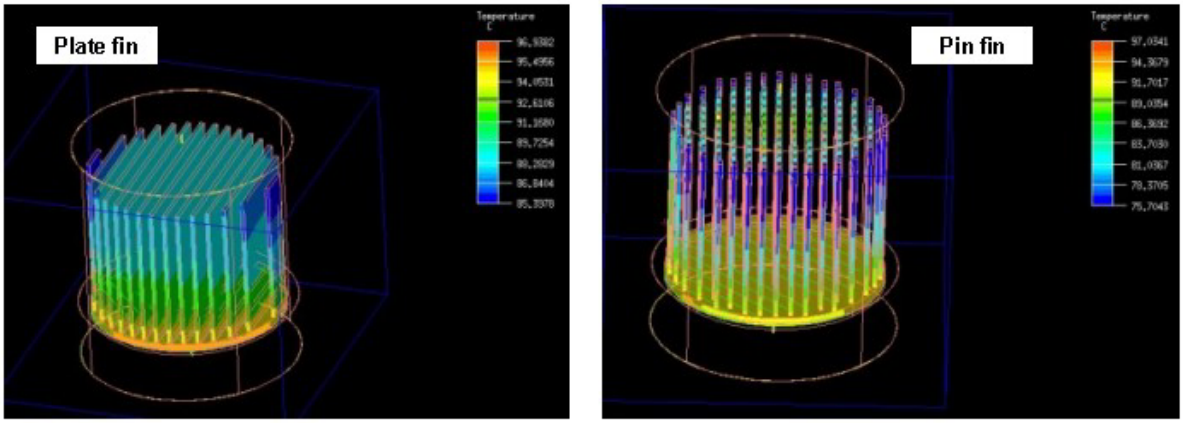

Figure 17. Comparison of plate fin and pin fin heat sink for LED light engine.

System level thermal management for LED lighting systems was discussed for a conceptual design. CFD models were created to understand the effect of the number, height and material of the fins. Radiation effects were included in these models. Significant radiation effects (15-25%) were seen in free convection applications. This is important since the heat transfer performance is typically poor for natural convection. A heat sink with a footprint area of 8 in^2 with fins 3” or taller as shown to remove 80 W and maintain a junction temperature of 120 °C.

SUMMARY AND CONCLUSIONS

Historical development of LEDs and future perspectives for replacing conventional, energy-inefficient, high lumen, lighting systems were discussed. Thermal management is a key technology for creating reliable, high lumen, LED systems. Package level and system level thermal management constructs the overall thermal architecture. A successful design should have low thermal resistance between the junction and the heat sink base, which relies on conduction heat transfer. This is followed by system level thermal management, which includes heat sinks and extended surfaces. Active or preferably passive cooling with air will be the predominant choice for LED based illumination systems. Although it is expected that a lot of new thermal challenges will arise in the development solid state lighting systems, conventional semiconductor thermal management technology will enable many techniques to be easily-transferred to SSL. However cost, longer life expectations, and tight thermal envelope constraints will drive custom thermal solutions for LED based lighting systems.

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